We claim:

1. A method of forming multiple spacer widths on a substrate, comprising:

(a) providing a substrate with isolation regions and a plurality of transistor regions including first, second and third transistor regions comprised of a dielectric layer on said substrate between said isolation regions;

(b) forming a gate electrode on said dielectric layer in each of said plurality of transistor regions;

(c) forming an oxide layer on the substrate and on the gate electrodes in said plurality of transistor regions;

(d) forming a first silicon nitride layer on the oxide layer in said first transistor region;

(e) forming a second silicon nitride layer on the first silicon nitride layer in said first transistor region and on the oxide layer in said second transistor region;

(f) forming a third silicon nitride layer on the second silicon nitride layer in the first and second transistor regions and on the oxide layer in the third transistor region; and

(g) etching through said first, second, and third silicon nitride layers and through said oxide layer to form spacers having a first width adjacent to the gate electrode on said first transistor region, spacers having a second width adjacent to the gate electrode on said second transistor region, and spacers having a third width adjacent to the gate electrode on the third transistor region.

2. The method of claim **1** wherein said etching step is performed by an anisotropic etching process.

3. The method of claim **1** wherein said first width is larger than said second width and said second width is larger than said third width.

4. The method of claim **3** further comprised of forming said oxide layer on a gate electrode in a fourth transistor region in step (c), forming a fourth silicon nitride layer on the third silicon nitride layer in said first, second, and third transistor regions and on the oxide layer in the fourth transistor region between steps (f) and (g), and wherein the etching step also forms spacers having a fourth width adjacent to said gate electrode in said fourth transistor region, said fourth width is less than said third width.

5. A method of forming multiple spacer widths on a substrate, comprising:

(a) providing a substrate with isolation regions and a plurality of transistor regions including first, second, and third transistor regions comprised of a dielectric layer on said substrate between said isolation regions;

(b) forming a first gate electrode on said dielectric layer in said first transistor region, a second gate electrode on said dielectric layer in said second transistor region, and a third gate electrode on said dielectric layer in said third transistor region, said first gate electrode having a greater thickness than said second gate electrode and said second gate electrode having a greater thickness than said third gate electrode;

(c) forming an oxide layer on the substrate and on the gate electrodes in said plurality of transistor regions; and

(d) etching said oxide layer to form spacers with a first width adjacent to said first gate electrode, spacers having a second width less than said first width adjacent to

said second gate electrode, and spacers having a third width less than said second width adjacent to said third gate electrode.

6. The method of claim **5** further comprised of forming a fourth gate electrode on said dielectric layer in a fourth transistor region before forming said oxide layer and wherein the thickness of the fourth gate electrode is less than the thickness of said third gate electrode and wherein etching said oxide layer forms spacers having a fourth width less than said third width adjacent to said fourth gate electrode.

7. The method of claim **5** further comprising the step of forming an anti-reflective coating (ARC) over said first and second gate electrodes before depositing said oxide layer wherein the thickness of said ARC over said second gate electrode is thinner than the thickness of said ARC over said first gate electrode.

8. The method of claim **7** wherein said ARC is comprised of silicon oxynitride that is deposited by a CVD or PECVD method and has a thickness between about 100 and 2000 Angstroms.

9. The method of claim **7** further comprised of removing said ARC after etching said oxide layer.

10. A method of forming multiple spacer widths on a substrate, comprising:

(a) providing a substrate with isolation regions and a plurality of transistor regions including first, second, and third transistor regions comprised of a dielectric layer on said substrate between said isolation regions;

(b) forming a first gate electrode on said dielectric layer in said first transistor region, a second gate electrode on said dielectric layer in said second transistor region, and a third gate electrode on said dielectric layer in said third transistor

region, said first gate electrode having a thickness equal to the thickness of said second gate electrode and said third gate electrode having a thickness less than the thickness of said first and second gate electrodes;

(c) forming an oxide layer on said substrate in the plurality of transistor regions;

(d) forming a first silicon nitride layer on said oxide layer in said first transistor region;

(e) forming a second silicon nitride layer on said first silicon nitride layer in said first transistor region and on said oxide layer in said second and third transistor regions; and

(f) etching through said silicon nitride layers and through said oxide layer to form spacers having a first width adjacent to said first electrode, spacers having a second width less than said first width adjacent to said second gate electrode, and spacers having a third width less than said second width adjacent to said third gate electrode.

11. The method of claim **10** further comprised of forming a fourth gate electrode having a thickness less than the thickness of said third gate electrode on said dielectric layer in a fourth transistor region before forming said oxide layer, forming a third silicon nitride layer on said second silicon nitride layer in said first, second, and third transistor regions and on said oxide layer in the fourth transistor region, and wherein said etching forms spacers having a fourth width less than said third width adjacent to said fourth gate electrode.

12. A method of forming three different spacer widths on a substrate, comprising:

(a) providing a substrate with isolation regions and first, second, and third transistor regions comprised of a dielectric layer on said substrate between said isolation regions;

(b) forming a gate electrode on said dielectric layer in each of said first, second, and third transistor regions;

(c) forming a first oxide layer on the substrate and gate electrodes in said first, second, and third transistor regions wherein the thickness of said first oxide layer is thinner in said second and third transistor regions than in said first transistor region;

(d) etching said first oxide layer to form spacers having a first width adjacent to the gate electrode in said first transistor region and spacers having a second width less than said first width adjacent to the gate electrodes in said second and third transistor regions;

(e) forming a second oxide layer on the substrate and gate electrodes in said first, second, and third transistor regions wherein the thickness of said second oxide layer is thinner over said third transistor region than over said first and second transistor regions; and

(f) etching said second oxide layer to form spacers having a third width adjacent to the gate electrode in the first transistor region, spacers having a fourth width less than said third width adjacent to the gate electrode in the second transistor region, and spacers having a fifth width less than the fourth width adjacent to the gate electrode in the third transistor region.

13. The method of claim **12** wherein the first oxide layer is formed at a thinner thickness in certain transistor regions by masking transistor regions intended to have a thicker first oxide layer and then treating the unmasked transistor regions with a buffered HF solution.

14. The method of claim **12** wherein the second oxide layer is formed at a thinner thickness in certain transistor regions by masking transistor regions intended to have a thicker second oxide layer and then treating the unmasked transistor regions with a buffered HF solution.

15. A transistor structure, comprising:

(a) a semiconductor substrate having isolation regions and a plurality of transistor regions including first, second, and third transistor regions comprised of a dielectric layer formed on said substrate between said isolation regions;

(b) a gate electrode having a first thickness formed on said dielectric layer in said first transistor region, a gate electrode having a second thickness formed on said dielectric layer in said second transistor region, and a gate electrode having a third thickness formed on said dielectric layer in said third transistor region;

(c) oxide spacers having a width formed adjacent to said gate electrodes in said first, second, and third transistor regions; and

(d) silicon nitride spacers having a first width formed on said oxide spacers in said first transistor region, silicon nitride spacers having a second width less than said first width formed on said oxide spacers in said second transistor region, and silicon nitride spacers having a third width less than said second width formed on said oxide spacers in said third transistor region.

16. The transistor structure of claim **15** wherein said first thickness, said second thickness, and said third thickness are equivalent.

17. The transistor structure of claim **15** wherein said first thickness is equivalent to said second thickness and said first thickness is greater than said third thickness.

18. The transistor structure of claim **15** wherein the width of said oxide spacers is between about 10 and 1000 Angstroms.

19. The transistor structure of claim **15** wherein the first, second, and third widths of said silicon nitride spacers are between about 10 and 1000 Angstroms.

20. The transistor structure of claim **15** further comprised of a fourth gate electrode formed in a fourth transistor region, and oxide spacers formed adjacent to said fourth gate electrode, and silicon nitride spacers having a fourth width that is less than said third width formed on said oxide spacers.

21. A transistor structure, comprising:

(a) a semiconductor substrate having isolation regions and a plurality of transistor regions including first, second, and third transistor regions comprised of a dielectric layer formed on said substrate between said isolation regions;

(b) a gate electrode having a first thickness formed on said dielectric layer in said first transistor region, a gate electrode having a second thickness formed on said dielectric layer in said second transistor region, and a gate electrode having a third thickness formed on said dielectric layer in said third transistor region;

(c) oxide spacers having a first width formed adjacent to said gate electrode in the first transistor region, oxide spacers having a second width that is less than said first width formed adjacent to said gate electrode in the second transistor region, and oxide

spacers having a third width less than said second width formed adjacent to said gate electrode in the third transistor region.

22. The transistor structure of claim **21** wherein said first thickness is greater than said second thickness and said second thickness is greater than said third thickness.

23. The transistor structure of claim **21** wherein said first thickness, said second thickness, and said third thickness are equivalent.

24. The transistor structure of claim **21** wherein the width of said oxide spacers is between about 10 and 1000 Angstroms.

25. The transistor structure of claim **21** further comprised of a fourth gate electrode having a fourth thickness formed in a fourth transistor region and oxide spacers having a fourth width that is less than said third width formed adjacent to said fourth gate electrode.